WHAT IS CLAIMED IS:

1. A semiconductor memory device with a function of refreshing stored data, comprising:

a plurality of cell arrays, each composed of a predetermined number of rows of memory cells;

a plurality of sets of shift registers, an nth set of shift registers successively activating word line selection signals according to a given control signal, so as to refresh corresponding word lines of an nth cell array; and

a plurality of shift register controllers, an nth shift register controller providing the control signal to the nth set of shift registers when the nth cell array is being refreshed, the nth shift register controller forwarding the control signal to an (n+1)th set of shift registers when said refresh of the nth cell array is finished.

2. The semiconductor memory device according to claim 1, wherein the control signal that the nth shift register controller forwards to the (n+1)th set of shift registers is the word line selection signal used to refresh the last word line of the nth cell array.

3. The semiconductor memory device according to claim 1, wherein:

the word lines are hierarchically composed of main word lines and subordinate word lines; and

the nth shift register controller forwards the control signal to the (n+1)th set of shift registers when refresh of all the subordinate word lines of the nth cell array is finished.

4. The semiconductor memory device according to claim 1, wherein:

the word lines are hierarchically composed of main word lines and subordinate word lines; and

subordinate word line address specifying which subordinate word line to refresh is advanced each time the main word lines of the nth cell array are all refreshed.

5. The semiconductor memory device according to claim 1, wherein:

the plurality of cell arrays are divided into a plurality of groups of cell arrays; and

the semiconductor memory device further comprises a partial refresh controller that controls refresh of a limited refresh area of the plurality of groups in partial refresh mode.

6. The semiconductor memory device according to claim 5, wherein:

one of the plurality of cell arrays is designated

as a refresh start point; and

the partial refresh controller accepts a partial refresh request only when a refresh process has circulated among the cell arrays and returned to the refresh start point.

7. The semiconductor memory device according to claim 5, wherein, in the partial refresh mode, the partial refresh controller sets a refresh interval in inverse proportion to a ratio of the limited refresh area relative to an entire area of the cell arrays.

8. The semiconductor memory device according to claim 7, wherein the partial refresh controller exits from the partial refresh mode by expanding the refresh interval to the entire area of the cell arrays and then resetting the refresh interval to a normal interval.

9. The semiconductor memory device according to claim 4, wherein not all the subordinate word lines are selected in partial refresh mode.

10. The semiconductor memory device according to claim 1, wherein address selection of the cell arrays is locked by an external/internal address switching disable signal during a refresh process so that the cell arrays use internally generated address.

11. The semiconductor memory device according to claim 1, further comprising a plurality of redundancy circuits, one for each of the word lines, to repair a defect in the memory cells.

12. The semiconductor memory device according to claim 1, wherein data in said cell arrays are read out through shared sense amplifiers.